IN THE CLAIMS

1. (Currently Amended) A method of forming semiconductor devices having field ~~oxides~~ isolation layers in trenches, comprising:

providing a semiconductor substrate that includes a cell region and a high voltage region;

forming a pilot trench at a location in the high voltage region;

concurrently forming an upper trench, a bottom trench, and a trench in the cell region, the upper trench substantially centered at the location of the pilot trench, the bottom trench having a top at substantially the same level as a bottom surface of the upper trench, and the upper trench having a wider width than that of the bottom trench; and

~~forming an upper trench at a predetermined region of the semiconductor substrate and a bottom trench at a bottom surface of the upper trench; the upper trench having a wider width than the bottom trench; and~~

forming a field ~~oxide~~ isolation layer filling the bottom trench and the upper trench.

2. (Currently Amended) The method as claimed in claim 1, wherein concurrently forming the upper trench and bottom trench comprises:

~~forming an assistant trench at a predetermined region of the semiconductor substrate;~~

forming a trench mask layer on the semiconductor substrate having the pilot ~~assistant~~ trench;

forming an opening exposing the pilot ~~assistant~~ trench and a predetermined region of the semiconductor substrate at both sides of the pilot ~~assistant~~ trench by patterning the trench mask layer; and

forming the upper trench and the bottom trench by anisotropically etching the exposed bottom surface of the pilot ~~assistant~~ trench and the semiconductor substrate,

wherein the upper trench has substantially the same width as the opening and the bottom trench has substantially the same width as the pilot ~~assistant~~ trench.

3. (Currently Amended) The method as claimed in claim 2, further comprising forming a channel stop impurity-doped region in the semiconductor substrate apart from the bottom surface of the pilot ~~assistant~~ trench with a predetermined depth, wherein the bottom surface of the bottom trench is in contact with the channel stop impurity-doped region.

4. (Currently Amended) The method as claimed in claim 3, wherein the pilot ~~assistant~~ trench has substantially the same width as the channel stop impurity-doped region.

5. (Currently Amended) The method as claimed in claim 4, wherein forming the pilot ~~assistant~~ trench and the channel stop impurity-doped region comprises:

forming a[[n]] pilot ~~assistant~~ trench mask layer on the semiconductor substrate;

forming a[[n]] pilot ~~assistant~~ trench opening exposing a predetermined region of the semiconductor substrate by patterning the pilot ~~assistant~~ trench mask;

forming the [[an ]]pilot ~~assistant~~ trench by selectively etching the exposed semiconductor substrate;

forming a channel stop impurity-doped region in the semiconductor substrate apart from the bottom surface of the pilot ~~assistant~~ trench with a predetermined depth by implanting impurity ions using the patterned pilot ~~assistant~~ trench mask layer as a mask; and

removing the patterned pilot ~~assistant~~ trench mask layer.

6. (Currently Amended) The method as claimed in claim 3, wherein the pilot ~~assistant~~ trench has a wider width than the channel stop impurity-doped region.

7. (Currently Amended) The method as claimed in claim 6, wherein forming the channel stop impurity-doped region comprises:

forming an ion-implantation mask layer on the semiconductor substrate having the pilot ~~assistant~~ trench;

forming an ion-implantation opening having a narrower width than the pilot ~~assistant~~ trench and exposing a bottom predetermined region of the pilot ~~assistant~~ trench by patterning the ion-implantation mask layer;

forming a channel stop impurity-doped region in the semiconductor substrate apart from the bottom surface of the pilot ~~assistant~~ trench by implanting impurity ions using the patterned ion-implantation mask as a mask; and

removing the patterned ion-implantation mask.

8. (Currently amended) The method as claimed in claim 2, wherein forming the field ~~oxide~~ isolation layer comprises:

forming a field insulator filling the upper trench and the bottom trench on a surface of the semiconductor substrate;

planarizing the field insulator until the patterned trench mask layer is exposed; and removing the exposed trench mask layer.

9. (Currently Amended) The method as claimed in claim 1, wherein concurrently forming the upper trench and the bottom trench comprises:

forming ~~the~~ ~~an~~ upper trench at a predetermined region of the semiconductor substrate; and

concurrently forming the [[a]] bottom trench by selectively etching a bottom predetermined region of the pilot ~~upper~~ trench.

10. (Original) The method as claimed in claim 9, further comprising forming a channel stop impurity-doped region in the semiconductor substrate under the bottom trench, wherein the bottom surface of the bottom trench is in contact with the channel stop impurity-doped region.

11. (Currently Amended) The method as claimed in claim 9, wherein the pilot ~~assistant~~ trench has an identical or wider width than the channel stop impurity-doped region.

12. (Currently Amended) A method of forming semiconductor devices having field isolation layers in trenches comprising:

providing a semiconductor substrate having a first region and a second region;

forming a pilot trench in the second region;

forming in a single step, a first trench ~~at a predetermined region of the semiconductor substrate~~ in the ~~at the~~ first region and enlarging the pilot trench to form a second trench composed of an upper trench ~~at a predetermined region of the semiconductor substrate at the second region~~ and a bottom trench at the bottom of the upper trench; and

forming a first field ~~oxide~~ isolation layer filling the first trench and a second field ~~oxide~~ isolation layer filling the second trench,

wherein the first trench and the upper trench have identical depths from a surface of the semiconductor substrate and the upper trench has a wider width than the bottom trench.

13. (Currently Amended) The method as claimed in claim 12, wherein forming the first trench and the second trench comprises:

~~forming an assistant trench at a predetermined region of the semiconductor substrate at the second region;~~

forming a trench mask layer on the semiconductor substrate having the pilot ~~assistant~~ trench;

patterning the trench mask layer to form a first opening exposing a predetermined region of the semiconductor substrate at the first region and a second opening exposing the pilot ~~assistant~~ trench and a predetermined region of the semiconductor substrate at both sides of the pilot ~~assistant~~ trench at the second region; and

anisotropically etching the semiconductor substrate and a bottom surface of the pilot ~~assistant~~ trench exposed by the first opening and the second opening to form the first trench and the second trench-,

wherein the upper trench has substantially the same width as the second opening and the bottom trench has substantially the same width as the pilot ~~assistant~~ trench.

14. (Currently Amended) The method as claimed in claim 12 ~~14~~, wherein after forming the pilot ~~assistant~~ trench, the method further comprising forming a channel stop impurity-doped region in the semiconductor substrate apart from a bottom surface of the pilot ~~assistant~~ trench with a predetermined depth, wherein a bottom surface of the bottom trench is in contact with the channel stop impurity-doped region.

15. (Currently Amended) The method as claimed in claim 14, wherein the pilot ~~assistant~~ trench has substantially the same width as the channel stop impurity-doped region.

16. (Currently Amended) The method as claimed in claim 15, wherein forming of the pilot ~~assistant~~ trench and the channel stop impurity-doped region comprises:

forming a[[n]] pilot ~~assistant~~ trench mask layer on the semiconductor substrate;

forming a[[n]] pilot ~~assistant~~ trench opening exposing a predetermined region of the semiconductor substrate at the second region by patterning the pilot ~~assistant~~ trench mask layer;

forming the [[an ]]pilot ~~assistant~~ trench by etching the exposed semiconductor substrate;

forming a channel stop impurity-doped region in the semiconductor substrate apart from a bottom surface of the pilot ~~assistant~~ trench with a predetermined region by implanting impurity ions using the patterned pilot ~~assistant~~ mask layer as a mask; and

removing the patterned pilot ~~assistant~~ trench mask layer.

17. (Currently Amended) The method as claimed in claim 14, wherein the pilot ~~assistant~~ trench has a wider width than the channel stop impurity-doped region.

18. (Currently Amended) The method as claimed in claim 17, wherein forming the channel stop impurity-doped region comprises:

forming an ion-implantation mask layer on the semiconductor substrate having the pilot ~~assistant~~ trench;

forming an ion-implantation opening having a narrower width than the pilot ~~assistant~~ trench and exposing a predetermined region of a bottom surface of the pilot ~~assistant~~ trench by patterning the ion-implantation mask layer;

forming a channel stop impurity-doped region in the semiconductor substrate apart from a bottom surface of the pilot ~~assistant~~ trench with a predetermined depth by implanting impurity ions using the patterned ion-implantation mask layer as a mask; and

removing the patterned ion-implantation mask layer.

19. (Original) The method as claimed in claim 12, wherein forming the first trench and the second trench comprises:

forming a first trench at a predetermined region of the semiconductor substrate at the first region and an upper trench at a predetermined region of the semiconductor substrate at the second region; and

forming a bottom trench by selectively etching a predetermined region of a bottom surface of the upper trench.

20. (Original) The method as claimed in claim 19, further comprising forming a channel stop impurity-doped region under a bottom surface of the bottom trench, wherein the bottom surface of the bottom trench is in contact with the channel stop impurity-doped region.

21. (Original) The method as claimed in claim 20, wherein a width of the bottom trench is equal to or wider than that of the channel stop impurity-doped region.

22. (Currently Amended) A method of forming semiconductor devices having field oxides in trenches comprising:

providing a semiconductor substrate having a first region, a second region and a key region;

forming a[[n]] pilot ~~assistant~~ trench at a predetermined region of a semiconductor substrate at the second region and an initial key trench at a predetermined region of the semiconductor substrate at the key region;

forming a trench mask layer on a surface of the semiconductor substrate having the pilot ~~assistant~~ trench and the key trench;

patterning the trench mask layer to form a first opening exposing a predetermined region of the semiconductor substrate at the first region, a second opening exposing the pilot ~~assistant~~ trench and a predetermined region of the semiconductor substrate at both sides of the pilot ~~assistant~~ trench the second region and a key opening exposing the initial key trench and a predetermined region of the semiconductor substrate at the key region;

anisotropically etching the bottom surface of the pilot ~~assistant~~ trench and the exposed semiconductor substrate to form a first trench at the first region, a second trench composed of an upper trench at a surface of the semiconductor substrate at the second region and a bottom trench at a bottom surface of the upper trench, and a key trench composed of an upper key trench at a surface of the semiconductor substrate at the key region and a bottom key trench at a bottom surface of the upper key trench; and

forming a first field oxide in the first trench, a second field oxide in the second trench and a key field oxide in the key trench[[.]].

wherein ~~Wherein~~ the first trench, the upper trench and the upper key trench have identical depths from a surface of the semiconductor substrate, the upper trench has substantially the same width as the second opening and the bottom trench has substantially the same width as the pilot ~~assistant~~ trench.